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06ES32

Third Semester B.E. Degree Examination, June/July 2011
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least TWO questions from each part.*
2. Missing data may be assumed suitably.

PART – A

1 a. Define the following pertaining to the diode:
i) Dynamic resistance ii) Diffusion capacitance and iii) Reverse recovery time. **(06 Marks)**

b. Discuss the approximate and piecewise linear model of a diode. **(06 Marks)**

c. Sketch the output voltage $v_0(t)$ for the circuit shown in Fig.Q1(c), if $v_i(t) = 50 \sin\omega t$. Assume diodes D_1 and D_2 as ideal. **(08 Marks)**

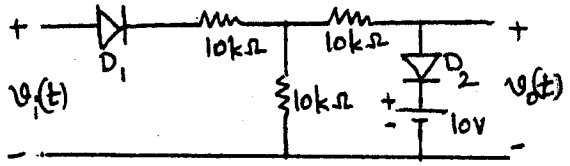

Fig.Q1(c)

2 a. What is biasing of a transistor? Explain the factors that affect selection of Q-point anywhere in the active region for the transistor to operate as an amplifier. **(06 Marks)**

b. What is bias stabilization? Discuss the stability of the operating point against variation in its parameters. **(06 Marks)**

c. Design a voltage divider bias circuit for the following specifications:
$V_{CC} = 15$ V, $V_{CE} = 7.5$ V, $I_C = 2$ mA, $S(I_{CO}) \leq 15$, $\beta = 100$ and $V_E = 1.5$ V. **(08 Marks)**

3 a. For the CE amplifier circuit derive the expression for A_I , Z_i , A_V and Y_o in terms of transistor h-parameters. **(10 Marks)**

b. For the circuit shown in Fig.Q3(b), find A_I , R_i , A_V and Z_o. The transistor h-parameters are $h_{ie} = 1$ kΩ, $h_{re} = 2\times10^{-4}$, $h_{fe} = 85$ and $h_{oe} = 2$ μʊ. **(10 Marks)**

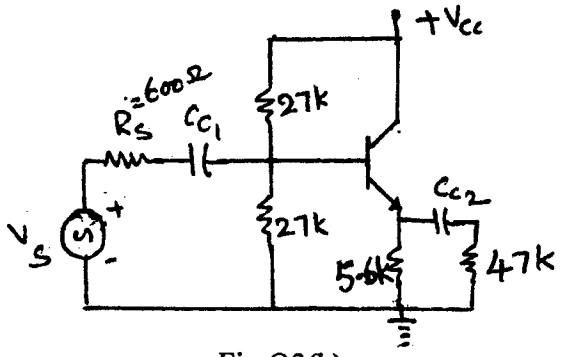

Fig.Q3(b)

4 a. Derive the expression for Miller's effect capacitances. **(06 Marks)**

b. Derive the expression for overall lower and higher cut off frequencies of multistage amplifier. **(06 Marks)**

c. At $I_C = 1$ mA and $V_{CE} = 10$V, a certain transistor data shows $C_c = C_{b'c} = 3$ pF, $h_{fe} = 200$ and $\omega_t = -500$ mrad/sec. Calculate g_m , $r_{b'e}$, $c_{b'e}$ and ω_β. **(08 Marks)**

PART – B

5 a. What is an emitter follower circuit? Discuss Darlington emitter following circuit. **(08 Marks)**

b. Fig.Q5(b) shows a circuit schematic of a feedback amplifier for which the parameters are $A = -2000$, $\beta = 1/150$, $R_s = R_E = 1\ k\Omega$, $R_C = 3\ k\Omega$, $h_{ie} = 2\ k\Omega$, $h_{fe} = 200$ and $h_{re} = h_{oe} = 0$. Show that $v_i = -200\ [V_s - V_f]$. Calculate $A_{V_f} = \frac{V_0}{V_s}$ **(12 Marks)**

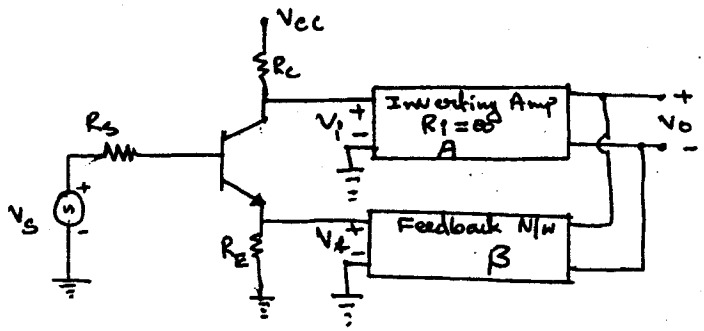

Fig.Q5(b)

6 a. Explain the operation of transformer coupled class A power amplifier. **(06 Marks)**

b. Show that maximum efficiency of the push pull class B power amplifier circuit is 78.5%. **(06 Marks)**

c. A complementary symmetry push pull amplifier is operated using $V_{CC} = \pm 10V$ and deliver power to a load $R_L = 5\ \Omega$. Calculate i) Maximum power output ii) Power rating of transistors iii) DC input at maximum power output. **(08 Marks)**

7 a. Obtain the Brakhausen criterion for operation of the oscillator using basic feedback circuit and hence, explain the operation of the oscillator. **(08 Marks)**

b. With neat circuit diagram, explain the operation of tuned oscillator. **(06 Marks)**

c. A crystal has L = 2H, C = 0.01 pF and R = 2 kΩ. Its mounting capacitance is 2 pF. Calculate its series and parallel resonating frequency. **(06 Marks)**

8 a. Explain the small signal model of the FET. **(04 Marks)**

b. Derive the expression for Z_i , Z_0 and A_v for FETSelf biased configuration (with R_S bypassed) **(06 Marks)**

c. For the Fig.Q8(c), $V_{GS} = -2.86V$ and $I_D = 4.56$ mA, find i) g_m ii) r_d iii) Z_i iv) Z_0 and v) A_V. Assume $I_{DSS} = 16$ mA, $V_p = -4V$ and $y_{os} = 25\ \mu\mho$. **(10 Marks)**

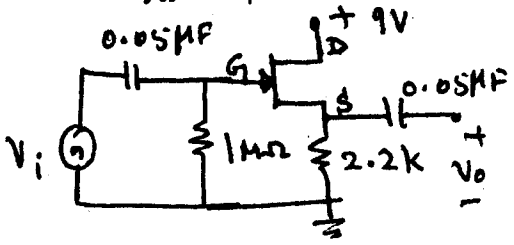

Fig.Q8(c)

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